DATA SHEET

TZA3017HW
30-3200 Mbits/s fibre optic transmitter

Objective specification
File under Integrated Circuits, IC19

2002 Jan 16

Philips
Semiconductors

PHILIPS

30-3200 Mbits/s fibre optic transmitter TZA3017HW

FEATURES

- Single 3.3 V power supply
- 1.5 W maximum power dissipation
- Supports SDH/SONET rates at 155.52, 622.08 and 2488.32 Mbits/s (including STM16/OC48 + FEC)
- Supports Gigabit Ethernet at 1250 and 3125 Mbits/s
- Supports Fibre Channel at 1062.5 and 2125 Mbits/s
- 16 : 1, 8 : 1 or 4 : 1 multiplexing ratio
- 10 : 1 multiplexing ratio for 8B/10B encoded protocols (e.g. Gigabit Ethernet)
- Rail-to-rail parallel inputs compliant with Positive Emitter Coupled Logic (PECL), Current-Mode Logic (CML) and Low Voltage Differential Signalling (LVDS)
- Supports co-directional and contra-directional clocking
- 4-stage FIFO providing large jitter tolerance on parallel interface
- Parity error detect, with programmable parity (odd or even)
- Loss Of Lock (LOL) indicator
- ITU-T compliant jitter generation
- CML data and clock outputs
- CML data and clock inputs for line loop back
- CML data and clock outputs for diagnostic loop back
- I²C-bus programmable.

Additional features with the I²C-bus

- Supports any line rate from 30 Mbits/s to 3.2 Gbits/s
- Programmable frequency resolution of 10 Hz
- Adjustable swing for CML data and clock outputs
- Adjustable polarity of all RF I/Os
- Clock versus data swap for optimum connectivity
- Programmable parallel bus order for optimum connectivity
- Adjustable LVPECL or CML output swing
- Reference frequency divide by 1, 2, 4 or 8.

APPLICATIONS

- Any optical transmission system with line rates between 30 Mbits/s and 3.2 Gbits/s
- Physical interface IC in transmit channels
- Transponder applications
- Dense Wavelength Division Multiplexing (DWDM) systems.

GENERAL DESCRIPTION

The TZA3017HW is a highly integrated optical network transmitter, comprising a clock synthesizer and a 16 : 1, 8 : 1 or 4 : 1 multiplexer (10 : 1 for 8B/10B encoded signals). The IC operates at any line rate between 30 Mbits/s and 3.2 Gbits/s. Additional RF inputs and outputs for loop mode connections are present. Using the I²C-bus gives the product a high configuration flexibility. The HTQFP100 package has excellent electrical and thermal properties.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3017HW	HTQFP100	plastic, heatsink thin quad flat package; 100 leads; body 14 × 14 × 1.0 mm	SOT638–1

BLOCK DIAGRAM

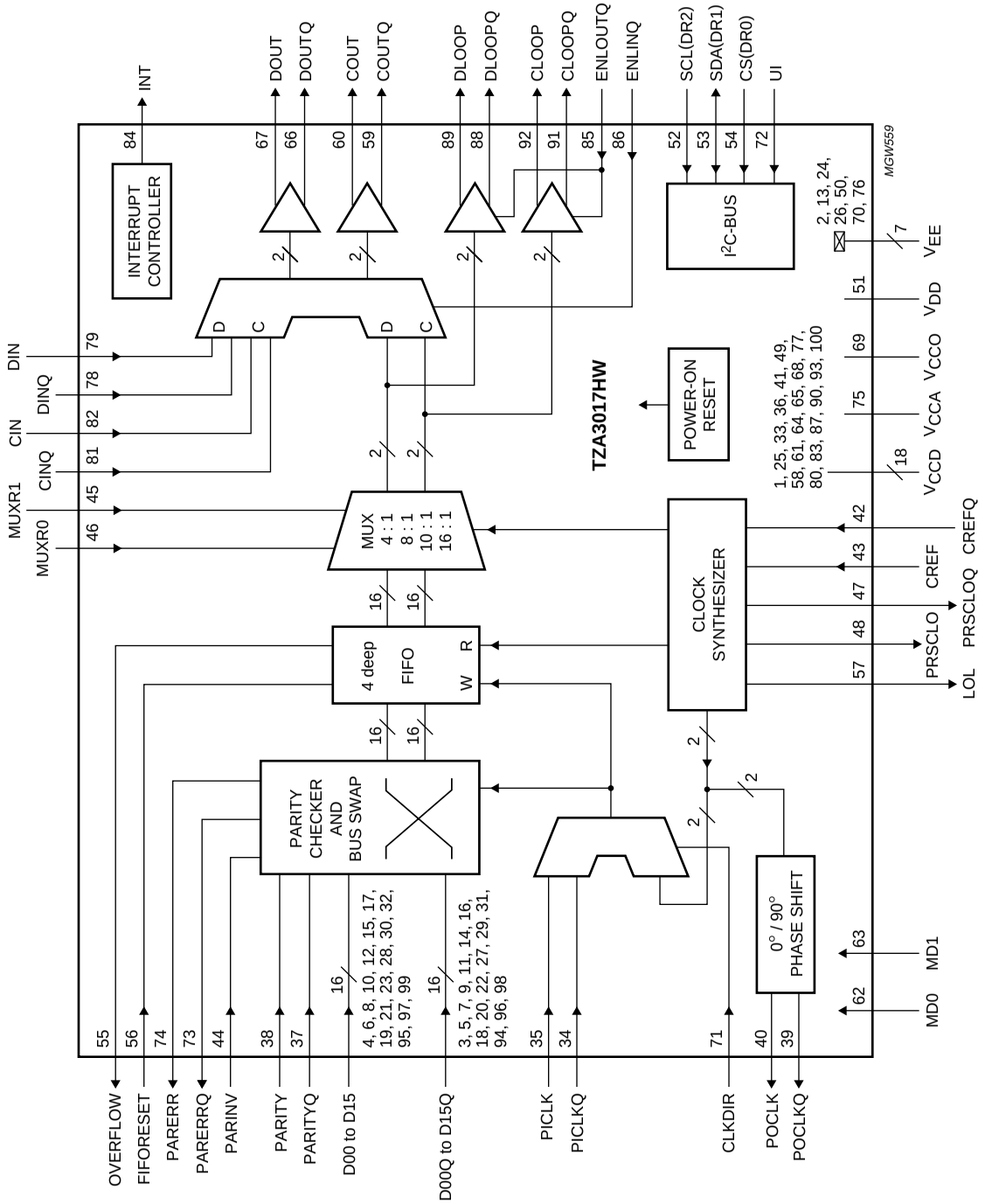


Fig.1 Simplified block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCD}	1	supply voltage (digital part)
V_{EE}	2	ground
D12Q	3	inverted parallel data input; bit 12
D12	4	non-inverted parallel data input; bit 12
D11Q	5	inverted parallel data input; bit 11
D11	6	non-inverted parallel data input; bit 11
D10Q	7	inverted parallel data input; bit 10
D10	8	non-inverted parallel data input; bit 10
D09Q	9	inverted parallel data input; bit 9
D09	10	non-inverted parallel data input; bit 9
D08Q	11	inverted parallel data input; bit 8
D08	12	non-inverted parallel data input; bit 8
V_{EE}	13	ground
D07Q	14	inverted parallel data input; bit 7
D07	15	non-inverted parallel data input; bit 7
D06Q	16	inverted parallel data input; bit 6
D06	17	non-inverted parallel data input; bit 6
D05Q	18	inverted parallel data input; bit 5
D05	19	non-inverted parallel data input; bit 5
D04Q	20	inverted parallel data input; bit 4
D04	21	non-inverted parallel data input; bit 4
D03Q	22	inverted parallel data input; bit 3
D03	23	non-inverted parallel data input; bit 3
V_{EE}	24	ground
V_{CCD}	25	supply voltage (digital part)
V_{EE}	26	ground
D02Q	27	inverted parallel data input; bit 2
D02	28	non-inverted parallel data input; bit 2
D01Q	29	inverted parallel data input; bit 1
D01	30	non-inverted parallel data input; bit 1
D00Q	31	inverted parallel data input; bit 0
D00	32	non-inverted parallel data input; bit 0
V_{CCD}	33	supply voltage (digital part)
PICLKQ	34	inverted parallel clock input
PICLK	35	non-inverted parallel clock input
V_{CCD}	36	supply voltage (digital part)
PARITYQ	37	inverted parity input
PARITY	38	non-inverted parity input
POCLKQ	39	inverted parallel output clock
POCLK	40	non-inverted parallel output clock
V_{CCD}	41	supply voltage (digital part)
CREFQ	42	inverted reference clock input
CREF	43	non-inverted reference clock input
PARINV	44	parity invert input (odd or even)
MUXR1	45	select MUX ratio
MUXR0	46	select MUX ratio
PRSCLOQ	47	inverted prescaler output signal
PRSCLO	48	non-inverted prescaler output signal
V_{CCD}	49	supply voltage (digital part)
V_{EE}	50	ground
V_{DD}	51	supply voltage (digital part)
SCL(DR2)	52	I^2C-bus serial clock (data rate select 2)
SDA(DR1)	53	I^2C-bus serial data (data rate select 1)
CS(DR0)	54	chip select (data rate select 0)
OVERFLOW	55	FIFO overflow alarm output
FIFORESET	56	FIFO reset input
LOL	57	loss of lock output
V_{CCD}	58	supply voltage (digital part)
COUTQ	59	inverted serial clock output
COUT	60	non-inverted serial clock output
V_{CCD}	61	supply voltage (digital part)
MD0	62	parallel data input termination mode select

SYMBOL	PIN	DESCRIPTION
MD1	63	parallel data input termination mode select
V_{CCD}	64	supply voltage (digital part)
V_{CCD}	65	supply voltage (digital part)
DOUTQ	66	inverted serial data output
DOUT	67	non-inverted serial data output
V_{CCD}	68	supply voltage (digital part)
V_{CCO}	69	supply voltage (clock generator)
V_{EE}	70	ground
CLKDIR	71	selection between co- and contra-directional input timing
UI	72	user interface selection
PARERRQ	73	inverted parity error output
PARERR	74	non-inverted parity error output
V_{CCA}	75	supply voltage (analog part)
V_{EE}	76	ground
V_{CCD}	77	supply voltage (digital part)
DINQ	78	inverted loop mode data input
DIN	79	non-inverted loop mode data input
V_{CCD}	80	supply voltage (digital part)
CINQ	81	inverted loop mode clock input
CIN	82	non-inverted loop mode clock input
V_{CCD}	83	supply voltage (digital part)
INT	84	interrupt output

SYMBOL	PIN	DESCRIPTION
ENLOUTQ	85	enable diagnostic loop back (active LOW)
ENLINQ	86	enable line loop back (active LOW)
V_{CCD}	87	supply voltage (digital part)
DLOOPQ	88	inverted loop mode data output
DLOOP	89	non-inverted loop mode data output
V_{CCD}	90	supply voltage (digital part)
CLOOPQ	91	inverted loop mode clock output
CLOOP	92	non-inverted loop mode clock output
V_{CCD}	93	supply voltage (digital part)
D15Q	94	inverted parallel data input; bit 15
D15	95	non-inverted parallel data input; bit 15
D14Q	96	inverted parallel data input; bit 14
D14	97	non-inverted parallel data input; bit 14
D13Q	98	inverted parallel data input; bit 13
D13	99	non-inverted parallel data input; bit 13
V_{CCD}	100	supply voltage (digital part)
V_{EE}	die pad	common ground plane

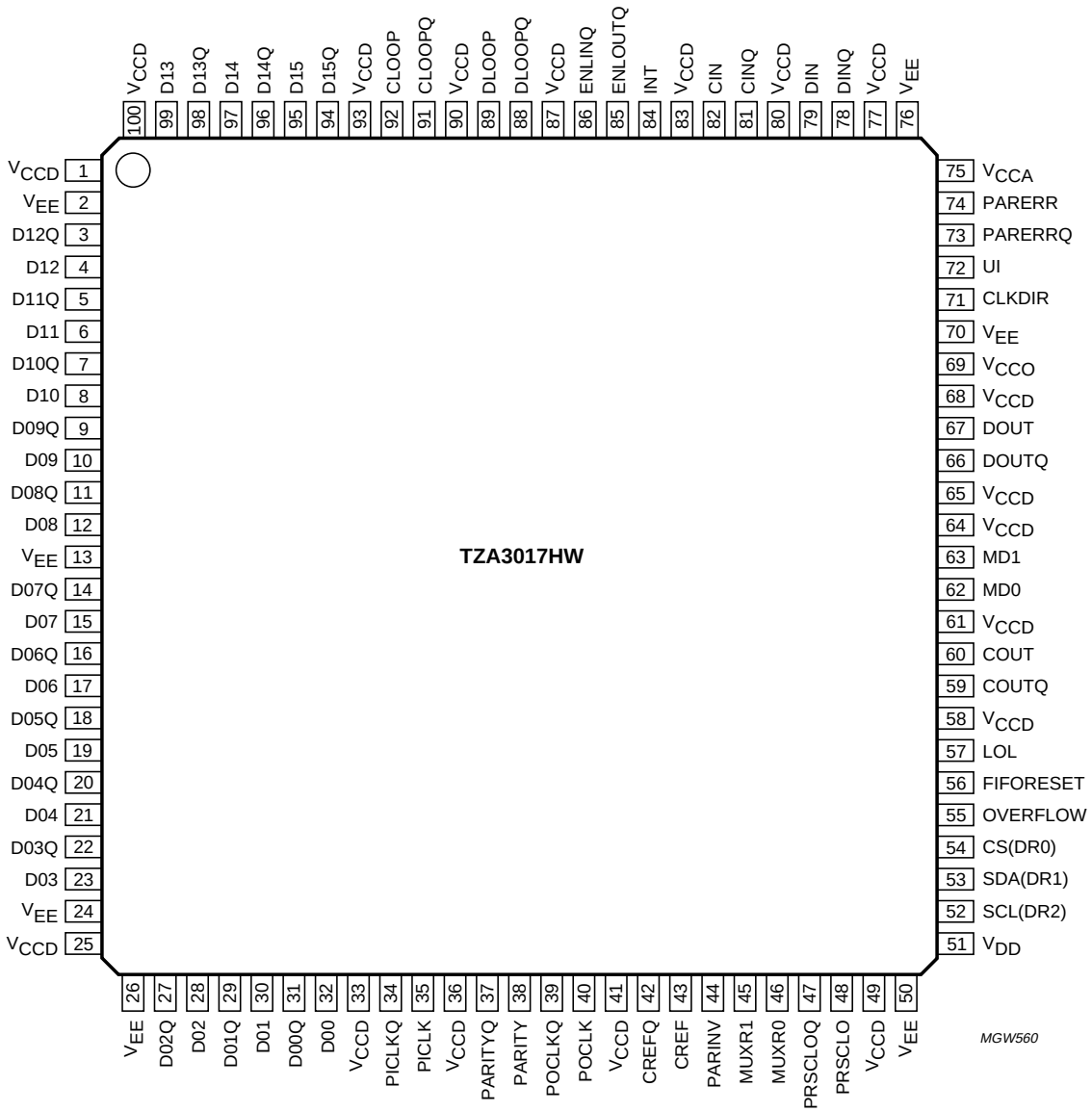


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TZA3017HW converts parallel data into a serial bit stream with a maximum line rate of 3.2 Gbits/s.
A multiplexing ratio of 4 : 1, 8 : 1 or 16 : 1 can be selected. For 8B/10B encoded protocols (e.g. Gigabit Ethernet), a multiplexing ratio of 10 : 1 is supported. The IC contains a clock synthesizer that synchronizes the internal oscillator to an external reference frequency.

Configuring the TZA3017HW by I²C-bus or external pins

The IC features two types of user interface: I²C-bus or direct programming of eight pre-defined modes. Interface selection is set by pin UI (user interface); see Table 1. The I²C-bus mode is operational if pin UI is left open or connected to V_{CC}. If pin UI is connected to V_{EE}, pins DR0, DR1 and DR2 are available for selection of eight pre-programmed modes.

Table 1 Truth table for UI

PIN UI	MODE	PIN 54	PIN 53	PIN 52
0	pre-programmed	DR0	DR1	DR2
1	I²C-bus control	CS	SDA	SCL

In I²C-bus mode, the chip is configured by using the I²C-bus connections (SDA and SCL). The Chip Select pin CS has to be HIGH during I²C-bus read or write actions. When pin CS is set LOW, the programmed configuration remains active, but signals SDA and SCL are ignored. In this way, all ICs in the application with the same I²C-bus addresses (e.g. other TZA3017) are individual accessible. The I²C-bus address is given in Table 2.

Table 2 I²C-bus address of the TZA3017HW

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	0	1	0	0	X

A detailed list of all I²C-bus registers and the meaning of their contents can be found in Chapter “I²C-bus registers”. Some functions in the TZA3017HW are controllable by using a pin or the I²C-bus. In these cases an extra I²C-bus bit, called I2C<pinname>, is available to set the programming precedence to the pin or the I²C-bus bit (default is selection by pin).

If no I²C-bus control is present in the application, the IC is applicable in the ‘pre-programmed mode’, but with reduced functionality. This mode allows the selection of eight commonly used bit rates or protocols.

If pin UI is connected to V_{EE}, the redefined pins DR0, DR1 and DR2 act as standard CMOS inputs that select any of the desired data rates given in Table 3.

Table 3 Truth table for pins DR2, DR1 and DR0 (UI = V_{EE})

PIN DR2	PIN DR1	PIN DR0	PROTOCOL	LINE RATE (Mbits/s)
LOW	LOW	LOW	STM1/OC3	155.52
LOW	LOW	HIGH	STM4/OC12	622.08
LOW	HIGH	LOW	STM16/OC48	2488.32
LOW	HIGH	HIGH	STM16 + FEC	2666.06
HIGH	LOW	LOW	GE	1250.00
HIGH	LOW	HIGH	10GE	3125.00
HIGH	HIGH	LOW	Fibre Channel	1062.50
HIGH	HIGH	HIGH	Fibre Channel	2125.00

The bit rates in Table 3 assume a reference frequency of 19.44 MHz applied to pins CREF and CREFQ.

After power-up, the TZA3017HW initiates a Power-On Reset (POR) sequence to restore the default settings of the I²C-bus registers, regardless of the programming mode. For the defaults; see Table 10.

Clock synthesizer

The clock synthesizer is a fractional N type of synthesizer, and consists of a Voltage Controlled Oscillator (VCO), several dividers, a Phase Frequency Detector (PFD), an integrated loop filter, a lock detection circuit and a prescaler output buffer; see Fig.3. The internal VCO is phase-locked to the reference clock signal provided at pins CREF and CREFQ. This frequency is typically 19.44 MHz.

Because of the 22 bits fractional N capability, any combination of line rate and reference frequency between 18 and 21 MHz is possible. The LSB (bit k[0]) of the fractional divider, should be set to logic 1 to avoid limit cycles. These are cycles of less than maximum length, which generate spurs in the frequency spectrum. This leaves 21 bits (k[21:1]) available for programming the fraction, allowing approximately 10 Hz of frequency resolution without altering the reference frequency.

To meet most transmission standards, the reference frequency should be very accurate. In order to be able to synthesize a clean RF clock, that is compliant with the most stringent jitter generation requirements, it should also be very clean in terms of phase noise; see Section “Jitter performance”.

All parts of the Phase-Locked Loop (PLL) are internal; no external components are required. This allows for easy application.

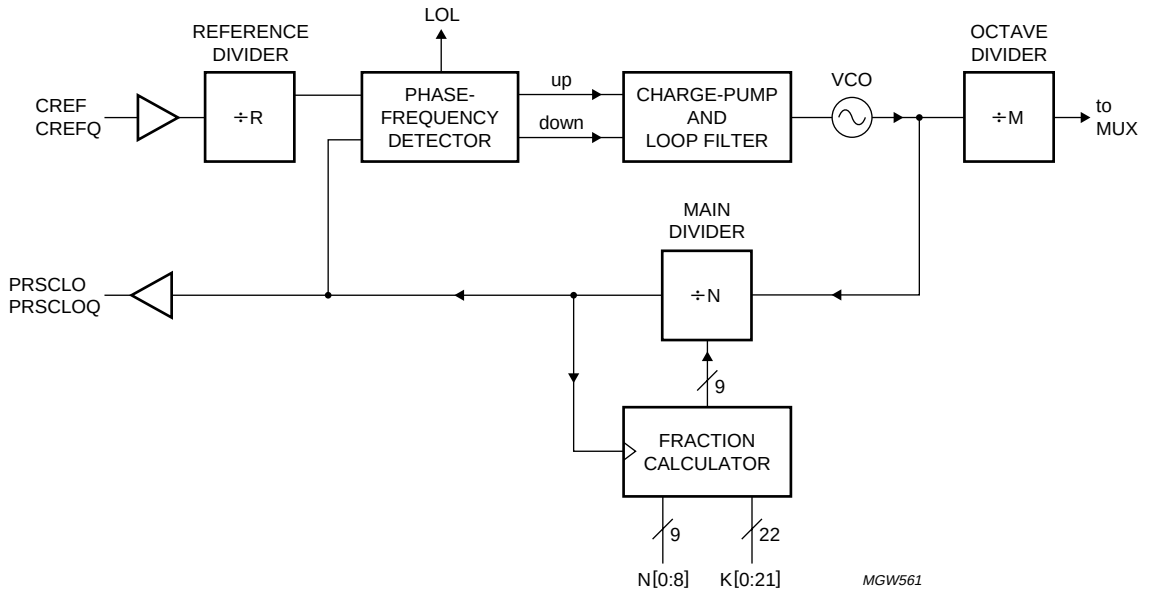


Fig.3 Schematic diagram of the clock synthesizer.

Programming the clock synthesizer

Programming the clock synthesizer involves four dividers: the reference (frequency) divider R, the main divider N, the fractional divider K and the octave divider M. The first step is to determine in which octave the desired bit rate fits. Figure 4 together with Tables 4 and 5 assists in finding the correct octave.

The value for R is usually 1; see Section “Programming the reference clock” for detailed information.

Once the octave and the reference frequency are known, the main division ratio N and the fractional part K, can be calculated according to the flowchart in Fig.5.

Four examples are given.

Table 4 Octave definition

OCTAVE	M	LOWEST BIT RATE (Mbits/s)	HIGHEST BIT RATE (Mbits/s)
0	1	1800	3200
1	2	900	1800
2	4	450	900
3	8	225	450
4	16	112.5	225
5	32	56.25	112.5
6	64	28.125	56.25

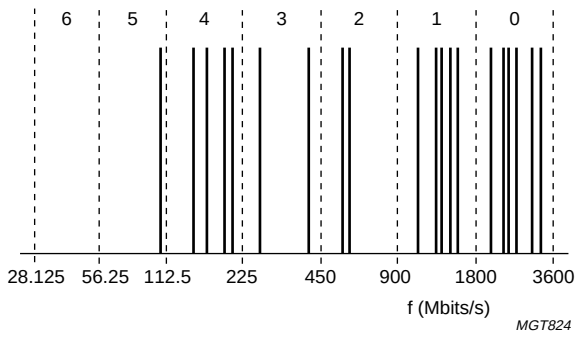


Fig.4 Commonly used line rates and allocation of octaves along a logarithmic bit rate scale.

Table 5 List of most common optical transmission protocols

PROTOCOL	LINE RATE (Mbits/s)	OCTAVE NUMBER
10GE	3125.00	0
2xHDTV	2970.00	0
STM16/OC48 +FEC	2666.06	0
STM16/OC48	2488.32	0
DV-6000	2380.00	0
Fibre Channel	2125.00	0
HDTV	1485.00	1
D-1 Video	1380.00	1
DV-6010	1300.00	1
Gigabit Ethernet	1250.00	1
Fibre Channel	1062.50	1
OptiConnect	1062.50	1
ISC	1062.50	1
STM4/OC12	622.08	2
DV-6400	595.00	2
Fibre Channel	425.00	3
OptiConnect	265.63	3
Fibre Channel	212.50	4
ESCON/SBCON	200.00	4
STM1/OC3	155.52	4
FDDI	125.00	4
Fast Ethernet	125.00	4
Fibre Channel	106.25	5

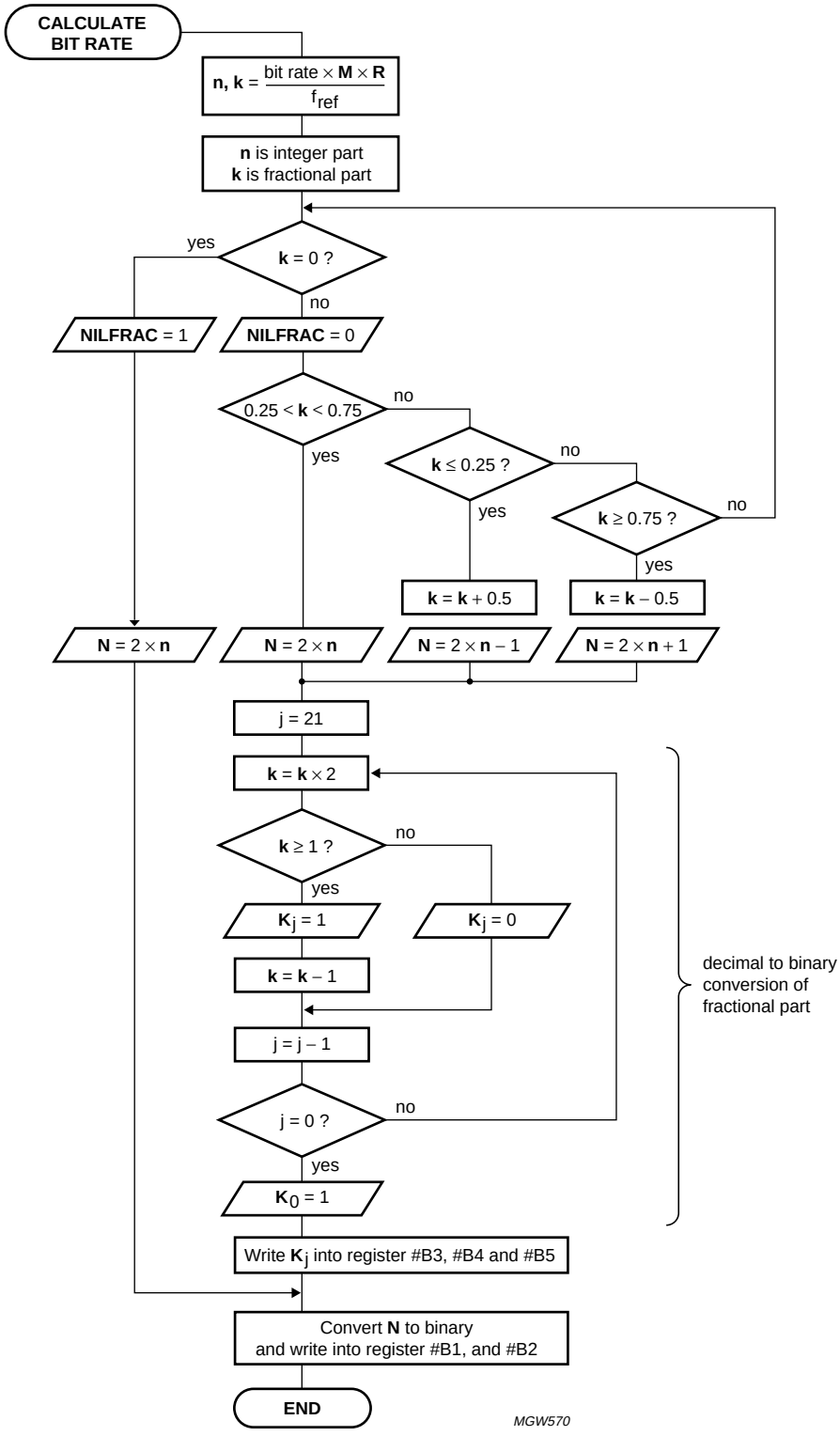


Fig.5 Flowchart to calculate N and K for the required bit rate.

Example 1: An SDH or SONET link has a line rate of 2488.32 Mbits/s (STM16/OC48) and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF and CREFQ is 77.76 MHz. This means that the reference division R needs to be 4; see Section “Programming the reference clock”. The values of **n** and **k** can be calculated from the flowchart: $n = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2488.32\ \text{Mbits/s} \times 1 \times 4}{77.76\ \text{MHz}} = 128$

Since **k** = 0 in this example, no fractional functionality is required, and bit NILFRAC should be logic 1 (register B3H). **N** = 2 × **n** and no correction is required. Consequently the appropriate values are: R = 4 (register B6H), M = 1 (register B0H) and **N** = 256 (registers B1H and B2H).

Example 2: An SDH STM16 or SONET OC48 link with FEC, has a line rate of 2666.057143 Mbits/s (15/14 × 2488.32 Mbits/s) and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF and CREFQ is 38.88 MHz. This means that the reference division R, needs to be 2. Calculate **n** and **k** from the flowchart: $n = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2666.05714283\ \text{Mbits/s} \times 1 \times 2}{38.88\ \text{MHz}} = 137.1428571$

This means that **n** = 137, **k** = 0.1428571 and bit NILFRAC should be logic 0 (register B3H). Since **k** < 0.25, **k** is corrected to 0.6428571, while the corrected **N** becomes **N** = 273. Consequently the appropriate values are: R = 2 (register B6H), M = 1 (register B0H), **N** = 273 (registers B1H and B2H) and **K** = 10 1001 0010 0100 1001 0011 (registers B3H, B4H and B5H).

The FEC bit rate is usually quoted to be 2666.06 Mbits/s. Due to round off errors, this leads to a slightly different value for **k** than in the example.

Example 3: A fibre channel link has a line rate of 1062.50 Mbits/s and consequently fits in octave number 1, so M = 2. Suppose the reference frequency provided at pins CREF and CREFQ, is 19.44 MHz. This means that the reference division R needs to be 1. Calculate **n** and **k** from the flowchart:

$n = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{1062.50\ \text{Mbits/s} \times 2 \times 1}{19.44\ \text{MHz}} = 109.3106996$

This means that **n** = 109, **k** = 0.3107 and bit NILFRAC should be logic 0 (register B3H). Since **k** is between 0.25 and 0.75, **k** does not need to be corrected and **N** = 2 × **n** = 218. Consequently the appropriate values are: R = 1 (register B6H), M = 2 (register B0H) and **N** = 218 (registers B1H and B2H). **K** = 01 0011 1110 0010 1000 0001 (registers B3H, B4H and B5H).

Example 4: A non standard transmission link has a line rate of 3012 Mbits/s and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF and CREFQ, is 20.50 MHz. This means that the reference division R needs to be 1. Calculate **n** and **k** from the flowchart: $n = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{3012\ \text{Mbits/s} \times 1 \times 1}{20.50\ \text{MHz}} = 146.9268293$

This means that **n** = 146, **k** = 0.9268293 and bit NILFRAC should be logic 0 (register B3H). Since **k** is larger than 0.75, **k** needs to be corrected to 0.4268293 and **N** = 2 × **n** + 1 = 293. Consequently the appropriate values are: R = 1 (register B6H), M = 1 (register B0H) and **N** = 293 (registers B1H and B2H). **K** = 01 1011 0101 0001 0010 1011 (registers B3H, B4H and B5H).

If the I^2C-bus is not used, switching the clock synthesizer to eight pre-programmed line rates is possible by using pins DR0, DR1 and DR2; see Table 3.

Programming the reference clock

Normal operation in an SDH/SONET application assumes the use of a 19.44 MHz reference clock connected to pins CREF and CREFQ. However, the use of any reference frequency between 18 and 21 MHz is allowed.

By using the I²C-bus, a wider range of clock frequencies can be used by programming R through bits REFDIV in register B6H; see Table 6. Internally, the reference frequency is always divided to the lowest range, from 18 to 21 MHz. For SDH/SONET applications, this would be19.44 MHz.

Table 6 Truth table for the REFDIV bits

REFDIV	DIVISION FACTOR R	SDH/SONET REFERENCE FREQUENCY	REFERENCE FREQUENCY RANGE
00	1	19.44 MHz	18 to 21 MHz
01	2	38.88 MHz	36 to 42 MHz
10	4	77.76 MHz	72 to 84 MHz
11	8	155.52 MHz	144 to 168 MHz

Prescaler output

The prescaler output (PRSCLO and PRSCLOQ) is always a measure of the internal frequency of the clock synthesizer. It is the VCO frequency divided by the main division factor. If the synthesizer is in-lock, the frequency is equal to the reference frequency at CREF and CREFQ divided by R. This forms an accurate reference for another PLL. If needed, bit PRSCLINV from register C8H, can invert the output of the prescaler.

If no prescaler information is desired, bit PRSCLEN from the same register can disable the output. Apart from these settings, the type of output, the termination mode and the signal amplitude can be set. These parameters follow the settings of the parallel multiplexer output clock (POCLK and POCLKQ) and parity error output (PARERR and PARERRQ). For programming details, see Section “Configuring the parallel bus”.

Loss Of Lock (LOL)

During normal operation, the Loss Of Lock output (pin LOL) should be LOW. In this event the clock synthesizer is in-lock, and the output frequency corresponds to the programmed value. If pin LOL goes HIGH, phase and/or frequency lock is lost, and the output frequency may deviate from the programmed value. The LOL condition is also available in I²C-bus registers INTERRUPT and STATUS; see Sections “Interrupt register” and “Status register”. On demand it generates an interrupt signal at pin INT; see Section “Interrupt generation”.

Jitter performance

The clock synthesizer of the TZA3017HW has been optimized for lowest jitter generation. For all SDH/SONET line rates, the jitter generation is compliant with ITU-T standard G.958, provided the reference clock is clean enough. For optimum jitter generation, the single sideband phase noise of the reference frequency should be less than −140 dBc/Hz, for frequencies greater than 12 kHz from the carrier. If the reference divider R is used, this requirement eleviates with approximately $20 \times \log (R)$.

Multiplexer

The multiplexer comprises a high-speed input register, a 4-bit deep First In First Out (FIFO) elastic buffer, a parity check circuit and the actual multiplexing tree.

Parallel bus clocking schemes

The TZA3017HW supports both co-directional and contra-directional clocking schemes for the parallel data bus; see Figs. 6 and 7. Pin CLKDIR or I²C-bus bit CLKDIR in register MUXCNF1 (register A1H), alters the clocking scheme. A HIGH level on pin CLKDIR or I²C-bus bit CLKDIR selects co-directional clocking, which is default. In the co-directional application, the clock is provided on pins PICLK and PICLKQ and the data on D00/D00Q to D15/D15Q. POCLK and POCLKQ is available if necessary, but can be disabled by I²C-bus bit POCLKEN (register A1H). In a contra-directional clock application, no clock is provided on pin PICLK. The clock that samples the input data on the parallel bus is an internal clock derived from POCLK. In this application, the part providing the parallel data has to be clocked with the POCLK/POCLKQ clock. In order to alleviate timing problems, the phase of POCLK, with respect to the internal clock, can be shifted in 90 degree steps. I²C-bus bit POCLKINV (180 degrees) together with bit POPHASE (90 degrees), set the phase shift; see Table 7. Both bits are located in register A1H.

Table 7 Truth table for the POCLKINV and POPHASE bits

POCLKINV	POPHASE	PHASE SHIFT
0	0	0°
0	1	90°
1	0	180°
1	1	270°

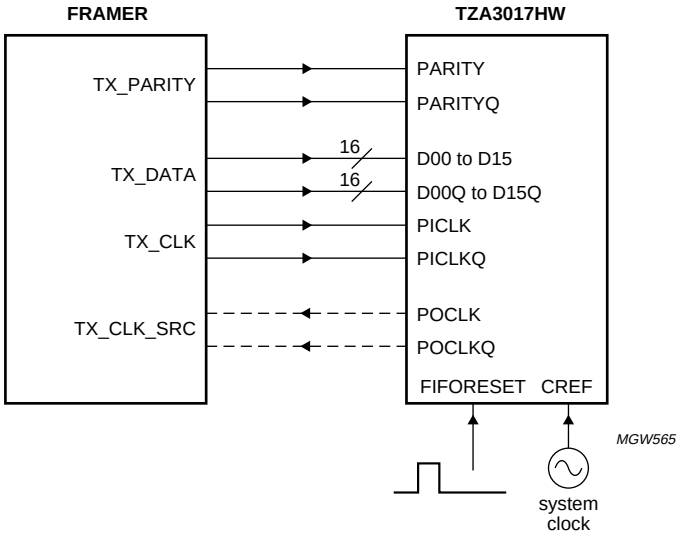


Fig.6 Co-directional clocking diagram.

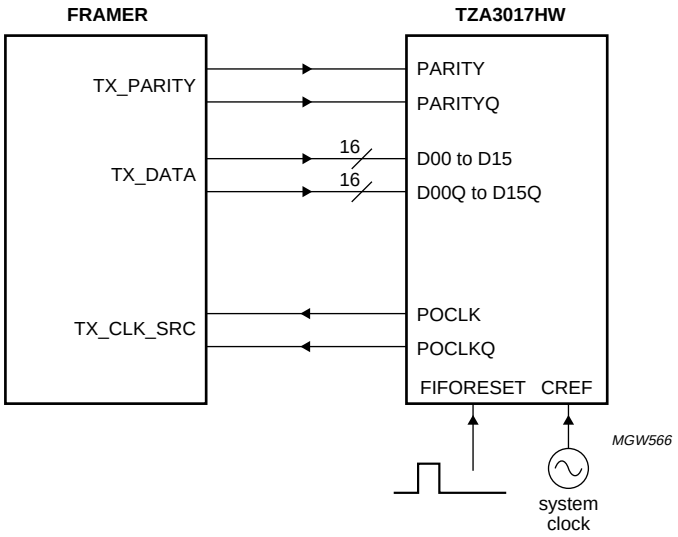


Fig.7 Contra-directional clocking diagram.

FIFO

In the co-directional clocking scheme, the input register samples the parallel bus data on the rising edge of PICLK/PICLKQ. The same clock writes this data into the FIFO. Data is retrieved from the FIFO by an internal clock, derived from the clock generator of the actual multiplexing tree. This provides for large jitter tolerance on the parallel interface; the FIFO absorbs momentary phase perturbations. Excessively large phase perturbations might stretch the elastic buffer to its limits, causing a FIFO over or underflow. Pin OVERFLOW and I^2C-bus registers INTERRUPT and STATUS indicate this situation; see Sections “Interrupt register” and “Status register”.
On demand it generates an interrupt signal at pin INT; see Section “Interrupt generation”.

The overflow alarm persists until the FIFO is reset by a HIGH level on pin FIFORESET or by I^2C-bus bit FIFORESET in register MUXCNF0 (register A2H). FIFORESET also initializes the FIFO. To fully benefit from the FIFO, it should be reset whenever there has been a Loss Of Lock condition, or when bit rates have changed.

The asynchronous FIFORESET signal is re-timed by the internal clock from the clock generator. Two clock cycles after FIFORESET has been made HIGH, the FIFO initializes. Two clock cycles after FIFORESET has been made LOW, the FIFO will be operational again. To initialize automatically, when an overflow has occurred, it is possible to connect pin OVERFLOW directly to pin FIFORESET.

Adjustable multiplexing ratio

Pins MUXR0 and MUXR1 or bits MUXR in I^2C-bus register MUXCNF1 (register A1H), configure the multiplexing ratio of the TZA3017HW. The parallel input bus is always centred around the middle (pin V_{EE}) for optimum layout connectivity. Table 8 lists the active inputs for the various multiplexing ratios. In I^2C-bus mode, the 16 : 1 ratio is default.

In 16 : 1 mode, D00/D00Q is the LSB, in 10 : 1 mode, D03/D03Q is the LSB, in 8 : 1 mode, D04/D04Q is the LSB and in 4 : 1 mode D06/D06Q is the LSB. Unused inputs are disabled.

For multiplexing ratios of 4 : 1, 8 : 1 and 16 : 1, the MSB is transmitted first. In 10 : 1 multiplexing mode, the LSB is transmitted first.

I^2C-bus bit BUSSWAP in register MUXCNF2 (A0H), changes the bus order. Bit BUSSWAP simply reverses the order of bits from MSB to LSB or vice versa, to allow for optimum layout connectivity.

The highest supported parallel bus speed is 400 Mbits/s. Therefore the 4 : 1 multiplexing ratio is only supported for line rates up to 1.6 Gbits/s.

Table 8 Setting the multiplexing ratio

PIN MUXR1	PIN MUXR0	BIT MUXR (REG 21H)	MULTIPLEXING RATIO	ACTIVE INPUT PINS
0	0	00	4 : 1	D06 to D09
0	1	01	8 : 1	D04 to D11
1	0	10	10 : 1	D03 to D12
1	1	11	16 : 1	D00 to D15 (all)

Parity checking

In order to check the integrity of the data provided on the parallel input bus, a parity checking function has been implemented in the IC. The calculated parity, based on the data currently on the bus, is compared to the expected parity provided at pins PARITY and PARITYQ. If these do not match, i.e. a parity error has occurred, the PARERR and PARERRQ outputs are HIGH during the next parallel bus clock period (PICLK period).

The type of parity, odd or even, can be set by pin PARINV or via I^2C-bus bit PARINV (register A0H). A LOW level corresponds with even parity, which is default for I^2C-bus bit PARINV.

Configuring the parallel bus

Several options exist that allow flexible configuration of the parallel bus and associated inputs and outputs.

For the outputs the configuration options are; output driver type, termination mode, output amplitude, signal polarity and selective enabling or disabling of various outputs. These options are set in registers MUXCNF1 (A1H) and IOCNF2 (C8H). The output pins affected by these registers are POCLK/POCLKQ, PARERR/PARERRQ and PRSCLO/PRSCLOQ.

Bit MFOUTMODE selects the CML or LVPECL output driver (default LVPECL). Bit MFOUTTERM sets the termination mode to standard LVPECL or floating termination, or, in case of CML, to DC or AC-coupled. The four MFS bits adjust the amplitude in all cases. The default output amplitude is 800 mV (p-p) single-ended.

Bit PDINV inverts the polarity of the parallel data and PICLKINV inverts the co-directional input clock, effectively shifting the clock edge by half a clock cycle, and changing the rising edge into a falling edge. This might resolve a parallel bus timing problem. Both bits are accessible in register MUXCNF2 (register A0H).

Rail-to-rail parallel data and clock inputs

The differential parallel data and clock inputs, D00/D00Q to D15/D15Q, PARITY/PARITYQ and PICLK/PICLKQ, handle any input swing with a minimum of 50 mV single-ended. The inputs accept any value between V_{EE} and V_{CC}, i.e. the input buffers are true rail-to-rail. The maximum current flowing into the pins and power dissipation generated by the input current, limit the maximum voltage swing. A differential hysteresis of 25 mV is implemented. I^2C-bus bit PIHYST in register MUXCNF0 (register A2H) switches the hysteresis. The default setting for the hysteresis is only active in LVDS mode.

In order to reduce the number of external components, internal termination is provided for the most common standards, such as LVPECL, CML and LVDS. Pins MD0 and MD1 determine the termination mode. Table 9 lists the supported options.

Table 9 Input termination mode selection

PIN MD1	PIN MD0	MODE	TERMINATION
0	0	floating	100 Ω differential
0	1	LVDS	100 Ω differential (hysteresis on)
1	0	CML	50 Ω to V_{CC}
1	1	LVPECL	50 Ω to V_{CC} – 2 V

Loop mode I/Os

As indicated in Fig.1, it is possible to use the IC for loop back purposes. A ‘line loop back’ is possible by setting pin ENLINQ to LOW. In this case, instead of taking the input from the multiplexer, the switch will select inputs DIN/DINQ and CIN/CINQ. Setting pin ENLOUTQ to LOW activates the ‘diagnostic loop back’ mode. In this case, the synthesized clock and serial data will be available both at the normal RF outputs (pins DOUT/DOUTQ and COUT/COUTQ) and at the loop mode output (pins DLOOP/DLOOPQ and CLOOP/CLOOPQ). I^2C-bus bits ENLOUT and ENLIN in register MUXCNF2 (register A0H) also sets these two loop modes.

Configuring the RF I/Os

The polarity of the individual serial data and clock I/Os can be inverted via the I^2C-bus. The position of the data and clock outputs (or inputs) can also be swapped. This solves connection problems with other ICs. Registers IOCNF0 (CBH) and IOCNF1 (CAH) program all RF I/O configurations.

When the RF input data and clock are swapped by means of bit CDINSWAP (register CAH), the signals present at pins CIN and CINQ are assumed to be data and the signals at pins DINQ and DIN are assumed to be clock. The same holds for swapping the RF outputs. By means of bit CDOUTSWAP (register CAH), normal mode data is present at pins COUTQ and COUT and clock at pins DOUTQ and DOUT. By means of bit CDLOOPSWAP (register CBH), the loop mode data output is present at pins CLOOPQ and CLOOP and clock at pins DLOOPQ and DLOOP.

I²C-bus bits DOUTENA and COUTENA (register CAH), independently disable normal mode outputs at pins DOUT/DOUTQ and COUT/COUTQ

The RF CML outputs have an (in 16 steps) adjustable signal amplitude between 62.5 mV (p-p) and 1000 mV (p-p) single-ended, controlled by bits RFS (register CBH). The default amplitude is 250 mV (p-p) single-ended. I²C-bus bit RFOUTTERM determines the termination scheme to be either DC or AC-coupled (DC-coupled is default).

CMOS control inputs

Most CMOS control inputs have an internal pull-up resistor. An open connection equals a HIGH input. Only the LOW state needs to be actively forced. This holds for pins UI, MUXR0, MUXR1, PARINV, CLKDIR, ENLOUTQ, ENLINQ, MD0, MD1, FIFORESET and CS. The same is true for pins DR0, DR1 and DR2 in pre-programmed mode (pin UI = LOW). In I²C-bus mode (pin UI = HIGH), pins SCL and SDA comply with the I²C-bus interface standard.

Power supply connections

Four separate supply domains (V_{DD}, V_{CCD}, V_{CCO} and V_{CCA}) provide isolation between the various functional blocks. Each supply domain should be connected to a common V_{CC} via separate filters. **All supply pins, including the exposed die pad, must be connected**. The die pad should be connected to ground with an as low as possible inductance. Since the die pad is also used as the main ground return of the chip, the connection should also have a low DC impedance. The voltage supply levels should be in accordance with the values specified in Chapters “Characteristics” and “Limiting values”.

All external components should be surface mounted devices, preferably of size 0603 or smaller. The components have to be mounted as closely to the IC as possible.

Interrupt register

The TZA3017HW INTERRUPT register (00H), reports the status of several alarm and mode indication flags; temperature alarm, loss of lock condition of the clock synthesizer and an overflow condition of the FIFO. An I²C-bus read action of register 00H, polls the interrupt register. The read action resets all status flags. If the alarm is still present, the interrupt flag is immediately set.

Status register

The TZA3017HW STATUS register (01H), holds the same content as the interrupt register, but reports the current status. i.e. without a memory function as used in the interrupt register. An I²C-bus read action of register 01H, polls the status register.

Interrupt generation

The TZA3017HW features a fully configurable interrupt generator, based on the interrupt flags (register 00H). Register INTMASK (register CCH) determines the masking of the status bits generating an interrupt.

The MSB of register INTMASK determines the output type of pin INT. The choices are standard CMOS output or open-drain outputs. The latter is the default value. I²C-bus bit INTPOL in the same register, determines the polarity of pin INT. The interrupt output is inverted as default, i.e. an interrupt will pull the output LOW. Together with the selected open-drain output, this set-up allows several receivers to be connected to a common interrupt wire. Only one 3.3 kΩ pull-up resistor is required. When an interrupt occurs, the status of the receiver is available at the INTERRUPT register (00H). An I²C-bus read action resets the interrupt register.

I²C-bus registers

Setting pin UI HIGH or leaving the pin open-circuit, allows I²C-bus programming. The I²C-bus registers can be accessed via the 2-wire I²C-bus interface (pins SCL and SDA), if pin CS (Chip Select) is HIGH during read or write actions. Table 10 shows the I²C-bus register list.

Table 10 I^2C-bus register list

ADDRESS	NAME	FUNCTION	DEFAULT	RANGE
00H	INTERRUPT	Interrupt register; see Table 11 for explanation		n.a.
01H	STATUS	Status register; see Table 12 for explanation		n.a.
A0H	MUXCNF2	Multiplexer configuration register 2; see Table 13 for explanation	0000 0000	n.a.
A1H	MUXCNF1	Multiplexer configuration register 1; see Table 14 for explanation	0110 1001	n.a.
A2H	MUXCNF0	Multiplexer configuration register 0; see Table 15 for explanation	0000 0000	n.a.
B0H	DIVCNF	Octave and loop mode configuration register; see Table 16 for explanation	0000 0000	n.a.
B1H	MAINDIV1	Main divider division ratio N (MSB); see Table 17 for explanation	0000 0001	(128 to 511)
B2H	MAINDIV0	Main divider division ratio N; see Table 18 for explanation	0000 0000	
B3H	FRACN2	Fractional divider division ratio K; see Table 19 for explanation	1000 0000	
B4H	FRACN1	Fractional divider division ratio K; see Table 20 for explanation	0000 0000	
B5H	FRACN0	Fractional divider division ratio K; see Table 21 for explanation	0000 0001	
B6H	SYNTHCNF	Synthesizer configuration register; see Table 22 for explanation	0000 0000	n.a.
C8H	IOCNF2	I/O configuration register 2; parallel outputs; see Table 23 for explanation	0010 1100	n.a.
CAH	IOCNF1	I/O configuration register 1; RF serial I/Os; see Table 24 for explanation	1100 0000	n.a.
CBH	IOCNF0	I/O configuration register 0; RF serial I/Os; see Table 25 for explanation	0000 0011	n.a.
CCH	INTMASK	Interrupt masking register; see Table 26 for explanation	0101 0000	n.a.

Table 11 Register INTERRUPT (address: 00H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Loss Of Lock (LOL)	LOL
							1	synthesizer out of lock (loss of lock condition)	
							0	synthesizer in lock	
				x	x	x			reserved
								Temperature alarm	TALARM
			1					junction temperature ≥ 140 °C	
			0					junction temperature < 140 °C	
								FIFO over or underflow:	OVERFLOW
		1						FIFO over or underflow occurred	
		0						FIFO normal operation	
0	0								reserved

Table 12 Register STATUS (address: 01H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Loss Of Lock (LOL)	LOL
							1	synthesizer out of lock (loss of lock condition)	
							0	synthesizer in lock	
				x	x	x			reserved
								Temperature alarm	TALARM
			1					junction temperature ≥ 140 °C	
			0					junction temperature < 140 °C	
								FIFO over or underflow	OVERFLOW
		1						FIFO over or underflow occurred	
		0						FIFO normal operation	
0	0								reserved

Table 13 Register MUXCNF2 (address: A0H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Parallel bus swapping	BUSSWAP
							1	D0 = MSB, D15 = LSB (swapped)	
							0	D15 = MSB, D0 = LSB (normal)	
								Parity checking	PARINV
						1		odd parity	
						0		even parity	
								Parity programming	I2CPARINV
					1			through I^2C-bus interface	
					0			through external pin PARINV	
								Parallel clock input polarity	PICLKINV
				1				inverted	
				0				normal	
								Parallel data input polarity	PDINV
			1					inverted	
			0					normal	
								Enable loop mode inputs	ENLIN
		1						loop mode inputs enabled	
		0						loop mode inputs disabled	
								Enable loop mode outputs	ENLOUT
	1							loop mode outputs enabled	
	0							loop mode outputs disabled	
								Loop mode control	I2CLOOPMODE
1								through I^2C-bus interface	
0								through external pins ENLINQ and/or ENLOUTQ	
0	0	0	0	0	0	0	0		default value

Table 14 Register MUXCNF1 (address: A1H, default value: 69H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Parallel clock output enable	POCLKEN
							1	enabled	
							0	disabled	
								Parallel clock output phase	POPHASE
						1		90° phase shift	
						0		0° phase shift	
								Parallel clock output polarity	POCLKINV
					1			inverted	
					0			normal	
								Parallel clock direction	CLKDIR
				1				co-directional clocking	
				0				contra-directional clocking	
								Parallel clock direction programming	I2CLKDIR
			1					through I^2C-bus interface	
			0					through external pin CLKDIR	
								Multiplexing ratio	MUXR
	1	1						16 : 1	
	1	0						10 : 1	
	0	1						8 : 1	
	0	0						4 : 1	
								Multiplexing ratio programming	I2CMUXR
1								through I^2C-bus interface	
0								through external pins MUXR0 and MUXR1	
0	1	1	0	1	0	0	1		default value

Table 15 Register MUXCNF0 (address: A2H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								FIFO reset	FIFORESET
							1	reset FIFO	
							0	normal mode	
								FIFO reset programming	I2CFIFORESET
						1		through I^2C-bus interface	
						0		through external pin FIFORESET	
								Parallel input hysteresis	PIHYST
					1			hysteresis with every input mode	
					0			hysteresis only in LVDS mode	
0	0	0	0	0					reserved
0	0	0	0	0	0	0	0		default value

Table 16 Register DIVCNF (address: B0H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Division ratio octave divider M; octave selection	DIV_M
					0	0	0	M = 1, octave number 0	
					0	0	1	M = 2, octave number 1	
					0	1	0	M = 4, octave number 2	
					0	1	1	M = 8, octave number 3	
					1	0	0	M = 16, octave number 4	
					1	0	1	M = 32, octave number 5	
					1	1	0	M = 64, octave number 6	
0	0	0	0	0					reserved
0	0	0	0	0	0	0	0		default value

Table 17 Register MAINDIV1 (address: B1H, default value: 01H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
0	0	0	0	0	0	0	N8	Division ratio divider N: N8 = MSB	DIV_N
0	0	0	0	0	0	0	1		default value

Table 18 Register MAINDIV0 (address: B2H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
N7	N6	N5	N4	N3	N2	N1	N0	Division ratio divider N: N0 = LSB	DIV_N
0	0	0	0	0	0	0	0		default value

Table 19 RegisterFRACN2(address: B3H, default value: 80H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
	x	K21	K20	K19	K18	K17	K16	Fractional divider K: K21 = MSB	DIV_K
								NILFRAC control bit (NF)	NILFRAC
1								no fractional N functionality	
0								fractional N functionality	
1	0	0	0	0	0	0	0		default value

Table 20 RegisterFRACN1(address: B4H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K15	K14	K13	K12	K11	K10	K9	K8	Fractional divider K	DIV_K
0	0	0	0	0	0	0	0		default value

Table 21 RegisterFRACN0(address: B5H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K7	K6	K5	K4	K3	K2	K1	K0	Fractional divider K: K0 = LSB	DIV_K
0	0	0	0	0	0	0	1		default value

Table 22 Register SYNTHCNF (address: B6H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
			0	0	0	0	0		reserved
								Synthesizer manual initialization	INITSYNTH
		1						toggle to initialize synthesizer	
		0						normal operation; auto initialize	
								Reference frequency divider	REFDIV
1	1							R = 8; Reference frequency = 155.52 MHz	
1	0							R = 4; reference frequency = 77.76 MHz	
0	1							R = 2; reference frequency = 38.88 MHz	
0	0							R = 1; reference frequency = 19.44 MHz	
0	0	0	0	0	0	0	0		default value

Table 23 Register IOCNF2 (address: C8H, default value: 2CH)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Parallel output signal amplitude	MFS
				0	0	0	0	minimum signal level; 60 mV (p-p)	
				1	1	0	0	default signal level; 800 mV (p-p)	
				1	1	1	1	maximum signal level; 1000 mV (p-p)	
								Prescaler output polarity	PRSCLINV
			1					inverted	
			0					normal	
								Prescaler output enable	PRSCLEN
		1						enabled	
		0						disabled	
								Parallel output termination	MFOUTTERM
	1							PECL mode: floating, CML mode: AC-coupled	
	0							PECL mode: standard, CML mode: DC-coupled	
								Parallel output mode	MFOUTMODE
1								CML; Current Mode Logic	
0								PECL; Positive Emitter Coupled Logic	
0	0	1	0	1	1	0	0		default value

Table 24 Register IOCNF1 (address: CAH, default value: C0H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Loop mode clock input polarity	CININV
							1	inverted	
							0	normal	
								Loop mode data input polarity	DININV
						1		inverted	
						0		normal	
								Loop mode input clock and data swap	CDINSWAP
					1			swapped clock and data input pairs	
					0			normal clock and data input	
								Clock output polarity	COUTINV
				1				inverted	
				0				normal	
								Data output polarity	DOUTINV
			1					inverted	
			0					normal	
								Output clock and data swap	CDOUTSWAP
		1						swapped clock and data output pairs	
		0						normal clock and data output	
								Clock output enable	COUTENA
	1							enabled	
	0							disabled	
								Data output enable	DOUTENA
1								enabled	
0								disabled	
1	1	0	0	0	0	0	0		default value

Table 25 Register IOCNF0 (address: CBH, default value: 03H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								RF serial output signal amplitude	RFS
				0	0	0	0	minimum signal level; 60 mV (p-p)	
				0	0	1	1	default signal level; 250 mV (p-p)	
				1	1	1	1	maximum signal level; 1000 mV (p-p)	
								Loop mode clock output polarity	CLOOPINV
			1					inverted	
			0					normal	
								Loop mode data output polarity	DLOOPINV
		1						inverted	
		0						normal	
								RF serial output termination	RFOUTTERM
	1							AC-coupled	
	0							DC-coupled	
								Loop mode output clock and data swap	CDLOOPSWAP
1								swapped clock and data output pairs	
0								normal clock and data output	
0	0	0	0	0	0	1	1		default value

Table 26 Register INTMASK (address: CCH, default value: 50H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Mask LOL signal	MLOL
							1	not masked	
							0	masked; note 1	
				0	0	0			reserved
								Mask temperature alarm	MTALARM
			1					not masked	
			0					masked; note 1	
								Mask OVERFLOW signal	MOVERFLOW
		1						not masked	
		0						masked; note 1	
								INT output polarity	INTPOL
	1							inverted; active LOW output	
	0							normal; active HIGH output	
								INT output mode	INTOUT
1								standard CMOS output	
0								open-drain output	
0	1	0	1	0	0	0	0		default value

Note

1. Signal is not processed by interrupt controller.

TZA3017HW WITHOUT USING I²C-BUS

Although the TZA3017HW is intended to be programmed via an I²C-bus, a lot of features can be accessed from external pins. This Chapter lists the functions of the TZA3017HW if the User Interface pin (UI) is LOW (no I²C-bus).

Features without the I²C-bus (UI = V_{EE}):

- 1 of 4 pre-programmed SDH/SONET bit rates; STM1/OC3, STM4/OC12, STM16/OC48, STM16/OC48 +FEC (DR2 to DR0)
- 1 of 4 pre-programmed bit rates; Fibre Channel, double Fibre Channel, Gigabit Ethernet, 10-Gigabit Ethernet (DR2 to DR0)
- 1 of 4 multiplexing ratios; 16 : 1, 8 : 1, 4 : 1 or 10 : 1 (MUXR1/MUXR0)
- Co-directional or contra-directional clocking scheme (CLKDIR)
- Loop mode serial input and output configuration (ENLINQ and ENLOUTQ)
- Even/odd parity checking (PARINV)
- LVPECL outputs on parallel interface with 1600 mV (p-p) differential signal (DC-coupled termination to V_{CC} − 2 V)
- CML serial RF outputs with 500 mV (p-p) differential signal (DC-coupled load)
- Loss Of Lock detection (LOL)
- FIFO overflow indication
- FIFO reset
- Temperature alarm (pin INT; open-drain).
- Supported reference frequency from 18 to 21 MHz.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCD}, V_{CCA}, V_{CCO}, V_{DD}	supply voltage	–0.5	+3.6	V
V_n	DC voltage on pins			
	D00 to D15, D00Q to D15Q, PICLK, PICLKQ, PARITY and PARITYQ	V_{CC} – 0.5	V_{CC} + 0.5	V
	POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO and PRSCLOQ	V_{CC} – 2.5	V_{CC} + 0.5	V
	UI, CS, SDA, SCL, MUXR0, MUXR1, CLKDIR, PARINV, FIFORESET, MD0, MD1, ENLOUTQ and ENLINQ	–0.5	V_{CC} + 0.5	V
	LOL and OVERFLOW	–0.5	V_{CC} + 0.5	V
	INT	–0.5	V_{CC} + 0.5	V
I_n	input current on pins			
	D00 to D15, D00Q to D15Q, PICLK, PICLKQ, PARITY and PARITYQ	–25	+25	mA
	CREF, CREFQ, CIN, CINQ, DIN and DINQ	–20	+20	mA
	INT	–2	+2	mA
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature	–40	+125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

In accordance with JEDEC standards JESD51-5 and JESD51-7.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient; 4 layer printed-circuit board in still air with 36 plated vias connected with the heatsink and the second and fourth ground layer in the PCB	16	K/W

CHARACTERISTICS

V_{CC} = 3.14 to 3.47 V; T_{amb} = –40 to +85 °C; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
I_{CCA}	analog supply current		–	2.2	2.4	mA
I_{CCD}	digital supply current	note 1	–	205	255	mA
		note 2	–	–	365	mA
I_{DD}	digital supply current		–	3	4	mA
I_{CCO}	oscillator supply current		–	29	38	mA
$I_{CC(tot)}$	total supply current	note 1	–	240	300	mA
		note 2	–	–	410	mA
P_{tot}	total power dissipation	note 1	–	0.79	1.05	W
		note 2	–	–	1.45	W
CMOS input; pins UI, DR0, DR1, DR2, CS, MUXR0, MUXR1, MD0, MD1, ENLINQ, ENLOUTQ, FIFORESET, PARINV and CLKDIR						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–155	µA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	–	–	1	µA
CMOS output; pins OVERFLOW, LOL and INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.2	–	V_{CC}	V
Open-drain output; pin INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	–	–	10	µA
Serial output; pins COUT, COUTQ, DOUT, DOUTQ, CLOOP, CLOOPQ, DLOOP and DLOOPQ						
$V_{o(p-p)}$	output voltage swing range (peak-to-peak value)	single-ended with 50 Ω external load; note 3	60	–	1000	mV
V_o	output voltage range		V_{CC} – 2	–	V_{CC}	V
Z_o	output impedance	single-ended to V_{CC}	80	100	120	Ω
t_r	rise time	20% to 80%	–	80	–	ps
t_f	fall time	80% to 20%	–	80	–	ps
$t_{d(C-D)}$	data-to-clock delay	between differential cross–overs	–100	–	100	ps
δ	duty cycle COUT/COUTQ	between differential cross–overs	40	50	60	%
f_{DR}	signal path data rate		30	–	3200	Mbits/s

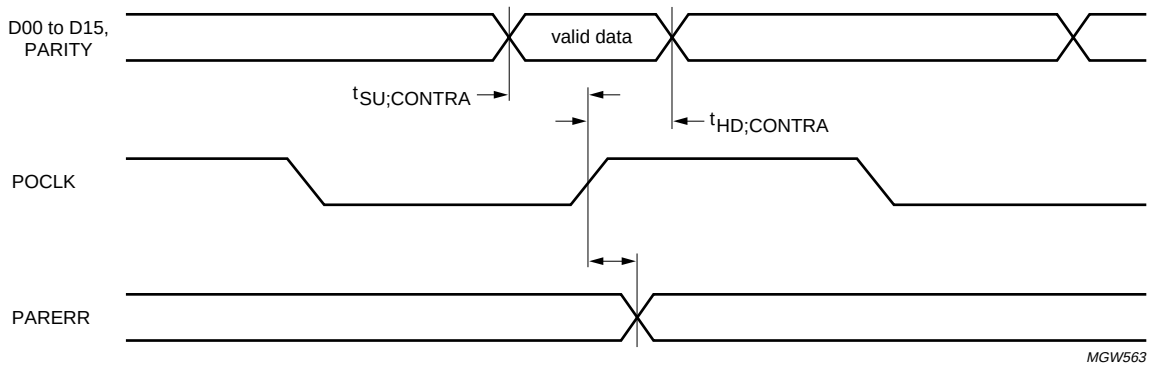
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Serial input; pins DIN, DINQ, CIN and CINQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	input voltage range		V_{CC} – 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
f_{DR}	signal path data rate		30	–	3200	Mbits/s
Parallel input (rail-to-rail); pins D00/D00Q to D15/D15Q, PARITY, PARITYQ, PICLK and PICLKQ						
V_I	input voltage range		V_{EE} – 0.25	–	V_{CC} + 0.25	V
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended	50	–	1000	mV
V_{hys}	input differential hysteresis	MD1 = LOW; MD0 = HIGH	25	–	–	mV
$Z_{i(diff)}$	differential input impedance	MD1 = LOW	80	100	120	Ω
$Z_{i(se)}$	single-ended input impedance	MD1 = HIGH	40	50	60	Ω
$V_{T(CML)}$	input termination voltage in CML mode	MD1 = HIGH; MD0 = LOW	–	V_{CC}	–	V
$V_{T(LVPECL)}$	input termination voltage in LVPECL mode	MD1 = HIGH; MD0 = HIGH	–	V_{CC} – 2	–	V
$t_{SU;CO}$	set-up time	co-directional clocking	–	–	0	ps
$t_{HD;CO}$	hold time	co-directional clocking	1000	–	–	ps
$t_{SU;CONTRA}$	set-up time	contra-directional clocking	–	–	tbf	ps
$t_{HD;CONTRA}$	hold time	contra-directional clocking	tbf	–	–	ps
δ	duty cycle PICLK/PICLKQ	between differential cross–overs	40	50	60	%
f_{par}	parallel bit rate		–	–	400	Mbits/s
CML output; pins POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO and PRSCLOQ						
$V_{o(p-p)}$	output voltage swing range (peak-to-peak value)	single-ended with 50 Ω external load; note 4	60	–	1000	mV
V_o	output voltage range		V_{CC} – 2	–	V_{CC}	V
Z_o	output impedance	single-ended to V_{CC}	80	100	120	Ω
t_r	rise time	20% to 80%	–	250	–	ps
t_f	fall time	80% to 20%	–	250	–	ps

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL output; pins POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO and PRSCLOQ						
V_{OH}	HIGH-level output voltage	50 Ω termination to V_{CC} – 2V	V_{CC} – 1.025	–	V_{CC} – 0.880	V
V_{OL}	LOW-level output voltage	50 Ω termination to V_{CC} – 2V	V_{CC} – 1.810	–	V_{CC} – 1.620	V
t_r	rise time	20% to 80%	–	250	–	ps
t_f	fall time	80% to 20%	–	250	–	ps
Reference frequency input; pins CREF and CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	input voltage range		V_{CC} – 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
Δf_{CREF}	reference clock frequency accuracy	SDH/SONET requirement	–20	–	+20	ppm
f_{CREF}	reference clock frequency	see Section “Programming the reference clock”	18	19.44	21	MHz
I²C-bus I/O pins; SCL and SDA						
V_{IL}	LOW-level input voltage		–0.5	–	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{hys}	hysteresis of Schmitt trigger inputs	note 5	$0.05V_{CC}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA; pin SDA open-drain	0	–	0.4	V
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance	note 5	–	–	10	pF
I²C-Timing						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{HD;STA}$	hold time for START condition		0.6	–	–	µs
$t_{SU;STA}$	set–up time for START condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set–up time		100	–	–	ns
$t_{SU;STO}$	set–up time for STOP condition		0.6	–	–	µs
t_r	SCL and SDA rise time	note 5	20	–	300	ns
t_f	SCL and SDA fall time	note 5	20	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{BUF}	bus free time between STOP and START		1.3	–	–	µs
C_b	capacitive load on each bus line		–	–	400	pF
t_{SP}	pulse width of allowable spikes	note 5	0	–	50	ns
V_{nL}	noise margin at LOW-level	note 5	$0.1V_{CC}$	–	–	V
V_{nH}	noise margin at HIGH-level	note 5	$0.2V_{CC}$	–	–	V
PLL characteristics						
$J_{gen(p-p)}$	jitter generation (peak-to-peak value)	STM1/OC3 mode; note 6				
		f = 500 Hz to 1.3 MHz	–	–	0.25	UI
		f = 12 kHz to 1.3 MHz	–	–	0.05	UI
		f = 65 kHz to 1.3 MHz	–	–	0.05	UI
		STM4/OC12 mode; note 6				
		f = 1 kHz to 5 MHz	–	–	0.25	UI
		f = 12 kHz to 5 MHz	–	–	0.05	UI
		f = 250 kHz to 5 MHz	–	–	0.05	UI
		STM16/OC48 mode; note 6				
		f = 5 kHz to 20 MHz	–	–	0.25	UI
		f = 12 kHz to 20 MHz	–	0.04	0.05	UI
		f = 1 to 20 MHz	–	–	0.05	UI

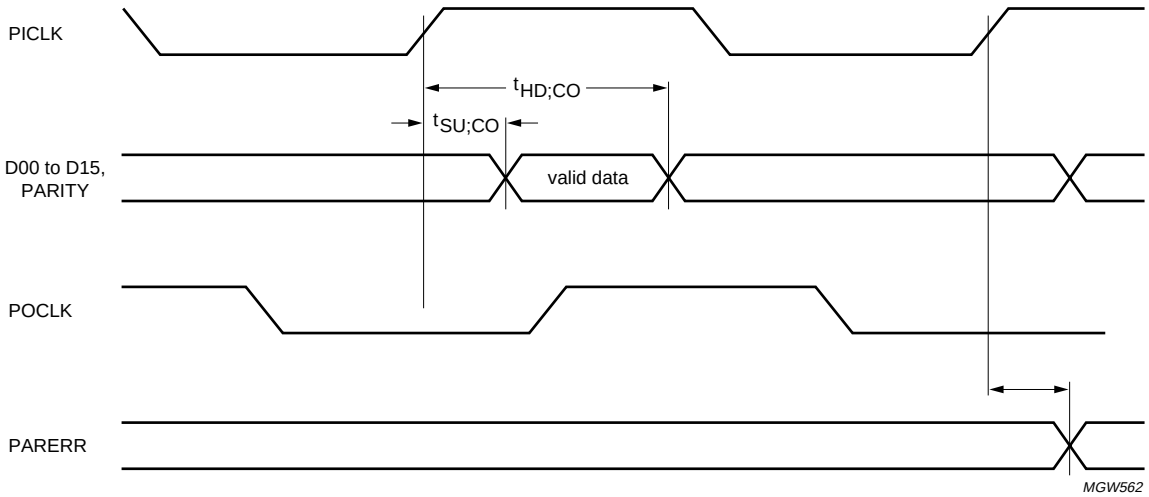
Notes

1. Outputs are not connected. Disabled loop modes, MUX ratio 16 : 1 and default output levels.
2. Outputs are not connected. Enabled loop modes, MUX ratio 16 : 1 and maximum output levels.
3. The output swing is (in 16 steps) adjustable between the min. and max. value, controlled by bits RFS in the I^2C-bus register CBH.
4. The output swing is (in 16 steps) adjustable between the min. and max. value, controlled by bits MFS in the I^2C-bus register C8H.
5. Guaranteed by design.
6. Reference frequency of 19.44 MHz, with a phase-noise of less than −140 dBc for frequencies of more than 12 kHz from the carrier.



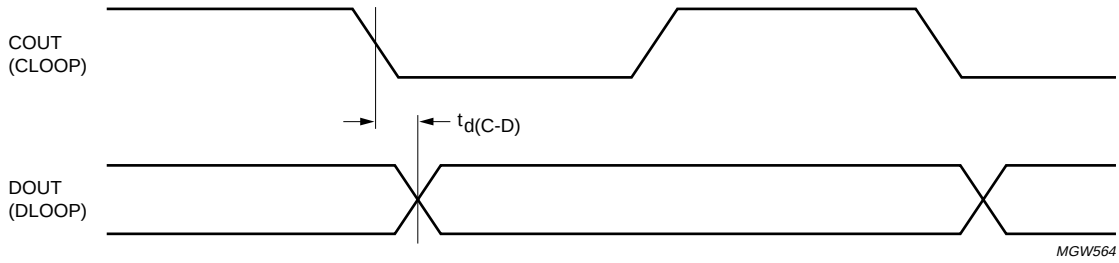
The timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Fig.8 Parallel bus contra-directional timing.



The timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Fig.9 Parallel bus co-directional timing.

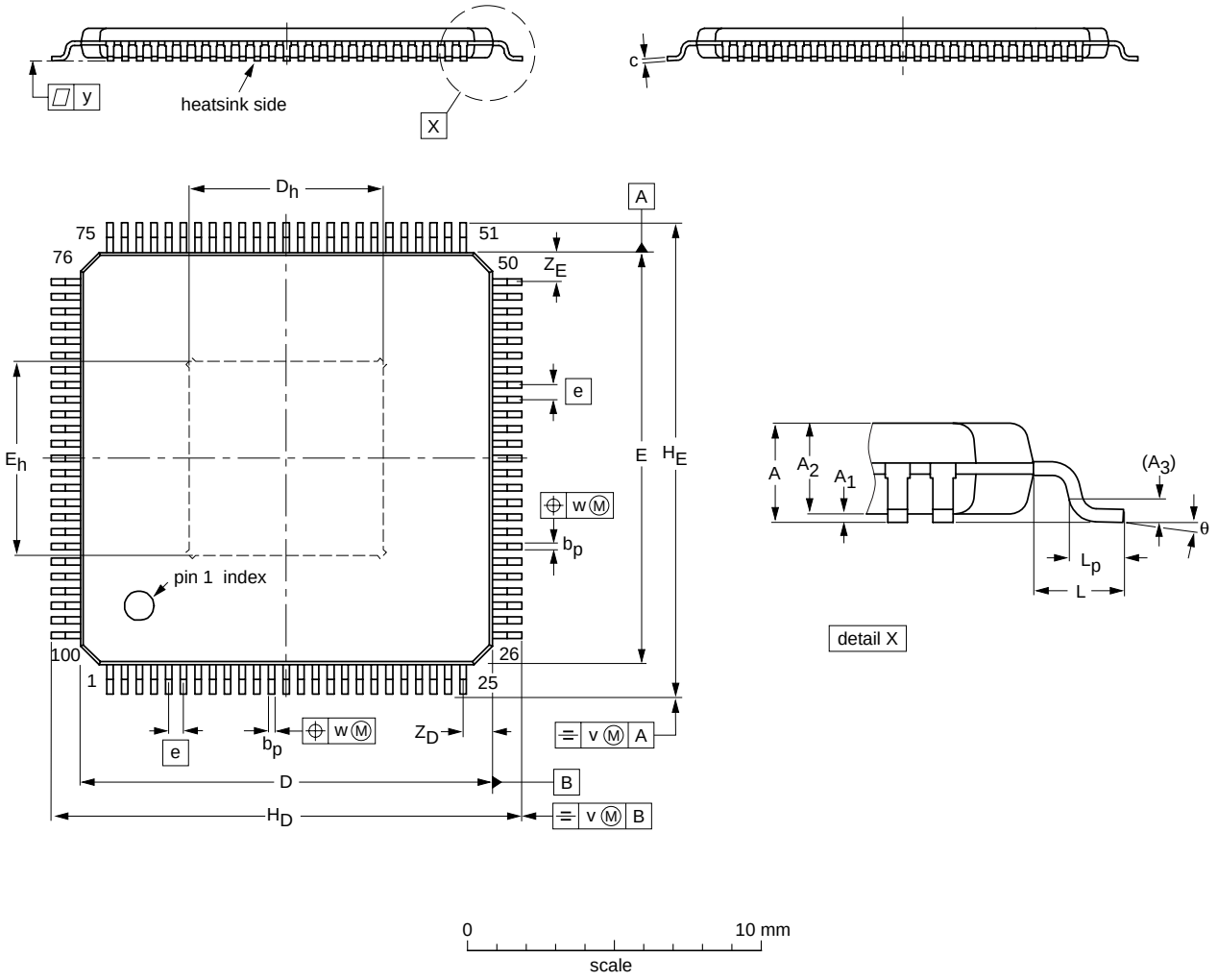


The timing is measured from the cross-over point of the reference signal to the cross-over point of the output.

Fig.10 RF output timing.

PACKAGE OUTLINE

HTQFP100: plastic, heatsink thin quad flat package; 100 leads; body 14 x 14 x 1.0 mm **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT638-1						01-03-30

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Printed in The Netherlands 403510/100/01/pp40 Date of release: 2002 Jan 16 Document order number: 9397 750 09169

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